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Horizon Robotics

Journey 3 Hardware Reference Design Errata

Rev. 0.4

Jan 28, 2021

Revision History

This section tracks the signi3ficant documentation changes that occur from release-to-release. The following table lists the technical content changes for each revision.

Revision	Date	Description
V 0.1	2020-11-12	Initial Draft for VAA ramp up rate issue and reset circuit
V0.2	2020-11-25	Add Design note for CNN power supply
V0.3	2021-01-11	Add 2.4 note for LPDDR4 power on/off sequence.
V0.4	2021-01-28	Add 2.5 USB Device mode Hot-plug Support

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1 Scope

This document describes the potential problems found during the verification of the Journey 3 DVB. The documents is applicable to the following Journey 3 DVB schematic and PCB layout revision.

Table 1-1 applicable reference design revision

Design	Filename	
Schematic	SC-2511-2-2A-DV-SM-02A-J3SOMLPDDR4-V1p0 SC-2511-2-2A-DV-SM-02A-J3SOMLPDDR4-V1p2	
PCB	SC-2511-2-2A-DV-SM-02A-J3SOMLPDDR4-V1p0 SC-2511-2-2A-DV-SM-02A-J3SOMLPDDR4-V1p2	

2 Schematic Design Note

2.1 DDR PHY power rail ramp up rate

Issue description:

Some of the Power rails of Journey 3 integrate a typical ESD protection circuit depicted by the following figure.

When VDD ramp up too fast (ESD transient), the RC delay circuit will keep Vrc low and Vg high, then Mesd will be opened to sink the ESD transient to VSS。

However, if normal power up event has too fast ramp up rate, it will mis-trigger the Mesd and has the very small potential to damage the Mesd after numerous power-up events.

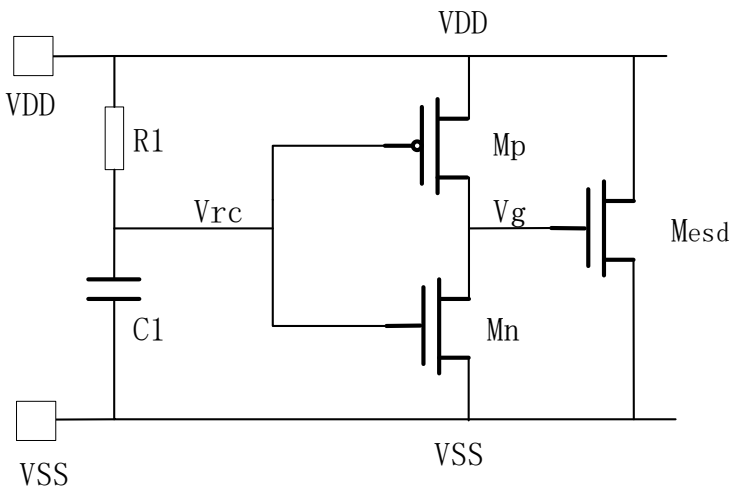

Figure 2-1 Journey 3 integrated ESD protection

The following table summarizes the requirements on the ramp up rate of Journey 3 's power rails.

Table 2-1 Journey 3 power ramp up rate requirements

Power rail	VDDQ_DDR VDDQLP_DDR VAA	VP_MIPI VPH_MIPI	VDD_USB VP_USB VPH_USB	EFUSE_VDD	ARMPLL_VDDPST ARMPLL_VDDHV ARMPLL_VDDREF	**Others**
Ramp up rate	<5mV/us	<100mV/us	<100mV/us	<60mV/us	No requirement	<18mV/us

Regarding the Journey 3 reference design, the failed power rail is VAA and PVT_VDDA_TAVDD. The actual measured ramp up rate is around 30mV/us.

Workaround:

There are two options to eliminate the potential risk.

- One option is to use a discrete LDO power supply which has < 5mv/us ramp up rate.
- The 2nd option is to use the following soft start circuit between the LDO output and VAA.

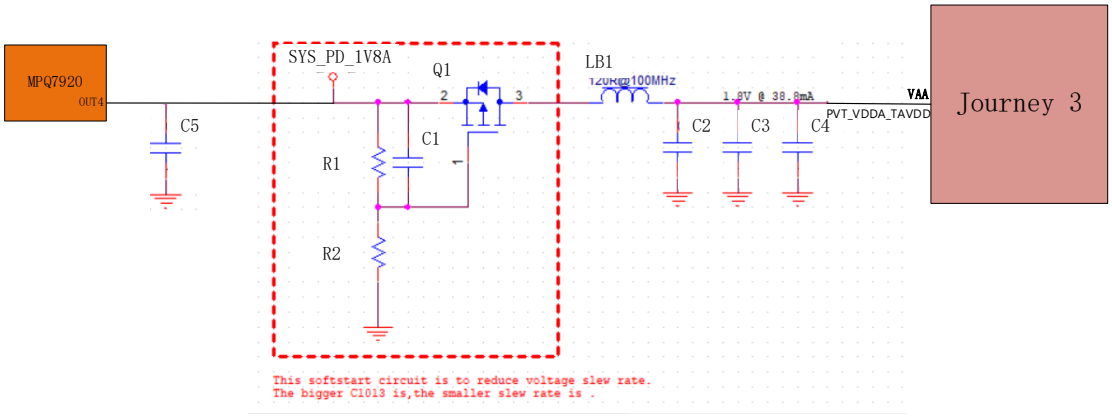

Figure 2-2 Ramp up rate control circuit

The following table describes the recommended value for passive components.

Table 2-2 passive components value recommendation

Ref.	Value	Vendor	Part number	Notes
C1	0.47uF	-	-	3
C2	10uF	-	-	-
C3	1uF	-	-	-
C4	0.1uF	-	-	-
C5	4.7uF	-	-	-
R1	100K Ohm	-	-	-

R2	10K Ohm	-	-	-
Q1	-	DIODES	DMG2305UXQ-7	1,2
LB1	120Ohm@100Mhz	-	-	-

Notes:

1. select Q1 with small Rdson (<200mOhm) and continuous Id drain current > 200mA
2. Make sure voltage feed into VAA still meets the ripple requirement (1.8V+/- 2.5%)
3. Adjust the value of C1 to achieve < 5mV/us ramp up rate.

2.2 Reset Circuit

Journey 3 needs external Power-On-Reset (POR) input through RSTN pin to reset the entire chip. The RSTN should be stable more than 10ms after all the power groups (1/2/3/4) achieve target value and 24MHz main clock is active and stable.

Figure 2-3 shows the recommended connection of external POR circuit.

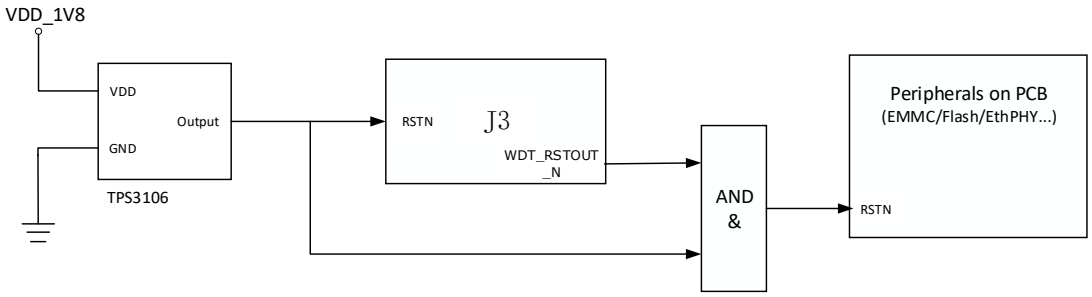

Figure 2-3 External POR reset circuit

WDT_RSTOUT_N is an active-low reset output signal and generated by J3 watchdog timeout event, it is used to reset peripherals on the board, EMMC, Flash, Ethernet PHY, etc.

***Note**:* WDT_RSTOUT_N signal needs to be sent to peripherals on the board especially memory devices (EMMC and Flash) and can't be sent back to J3's RSTN input signal via PCB trace.

2.3 CNN Power supply

Issue description:

Because Journey3's CNN behavior causes much higher di/dt (current variation over time) than other core power supply, the power supply to CNN core needs to have better transient load response performance. Otherwise, transient voltage drop will occur on VRM's output. Please check the following figure for this phenomenon.

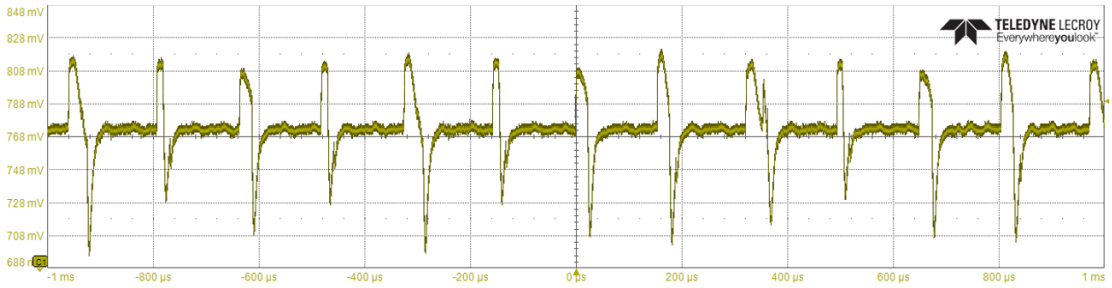

Figure 2-4 CNN Power supply transient voltage drop

Workaround:

To mitigate the potential problem caused by the voltage drop, there are 2 ways to improve the situation.

- First way is to choose a DCDC/PMIC with better transient load response performance, the following table depict a reference requirement for DCDC/PMIC transient load response.

Table 2-3 Reference DCDC/PMIC transient load response requirement

Transient load regulation	Undershoot	Overshoot
Under typical Cout **Iload (di/dt) = 2A/us**	Vout – 25mV	Vout + 25mV

- 2nd way is to increase Cout to BIGGER value if the PCB space could accommodate the extra component. The following table gives some reference part number which could be used. Customer could choose their own part number with enough capacitance and small ESR.

Table 2-4 Suggested Bulk Capacitor Part Number

Vendor	Part Number	Value	ESR	Qual
Panasonic	EEH-ZA1V101V	100uF	27 mΩ max	AEC-Q200
Panasonic	EEH-ZA1V221V	220uF	20 mΩ max	AEC-Q200

NOTE： Balance the DCDC/PMIC selection and Bulk capacitor selection to achieve the result depicted by following table. Be noted that the measurement should be done under customer typical scenario with BPU in maximum loading.

Table 2-5 CNN0/1 power supply

Power rail	Typical voltage	V peak to peak
VDD_CNN0/1	0.80V	*< 80mV (+/-5%)*

2.4 LPDDR4 Power on/off sequence

The LPDDR4 SDRAM has the specific power on/off sequence. The following requirements are extracted from DRAM datasheet and JEDEC specification JESD209-4C.

Voltage ramp

While applying power after Ta, VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

Table 2-6 LPDDR4 Power Ramp Sequence

After…	Applicable conditions
Ta is reached	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

Note:

1. Ta is the point when any power supply firstly reaches 300mV.

2. Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).

3. Tb is the point at which all supply and reference voltages are within their defined operating ranges.

4. Power ramp duration tINIT0 (Tb–Ta) must not exceed 20ms.

5. The voltage difference between any VSS and VSSQ must not exceed 100mV.

Power-Off Sequence

Table 2-7 LPDDR4 Power Off Sequence

Between…	Applicable conditions
Tx and Tz	VDD1 must be greater than VDD2
	VDD2 must be greater than VDDQ-200mV

Note:

1. Tx is the point where any power supply drops below the minimum value specified in the minimum DC Operating Condition.
2. Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Issue description:

J3 DVB does not meet this requirement. The power ramp and off sequence are as the Figure 2-5 and Figure 2-6.

Note: the yellow curve is 1.1V (VDDQ and VDD2), the blue curve is 1.8V (VDD1), the light green curve is 5V (input to the PMIC).

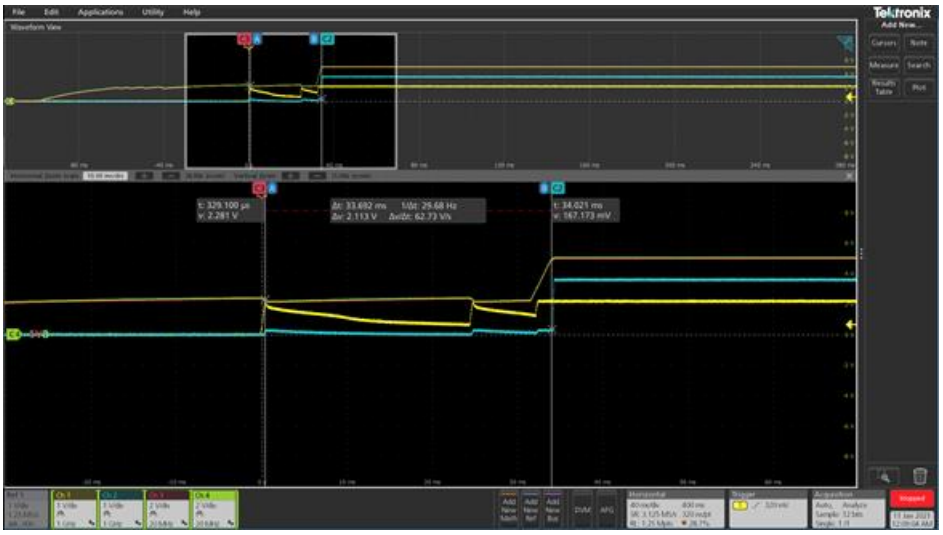

Figure 2-5 J3 DVB LPDDR4 Power Ramp up Sequence

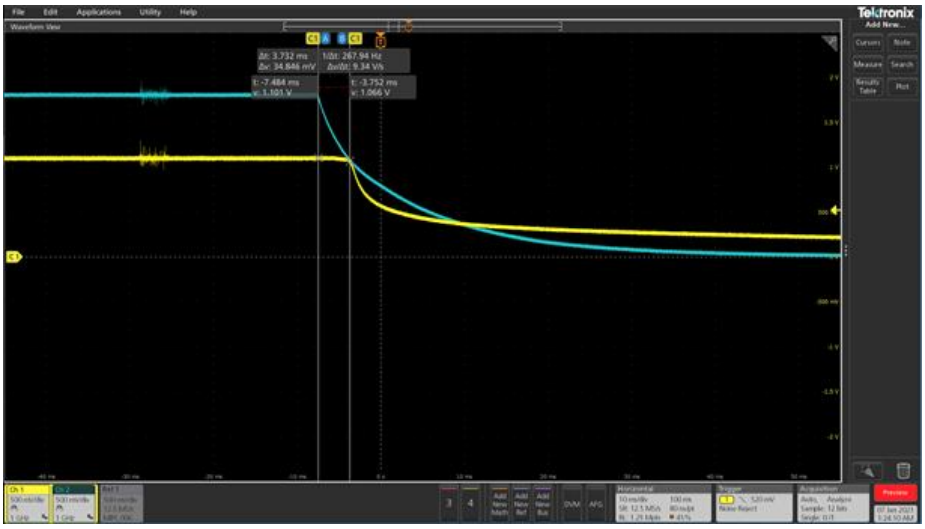

Figure 2-6 J3 DVB LPDDR4 Power Off Sequence

Workaround:

1. Change the EN input of MPQ2166 from 5V to 1.8V (VDD1).

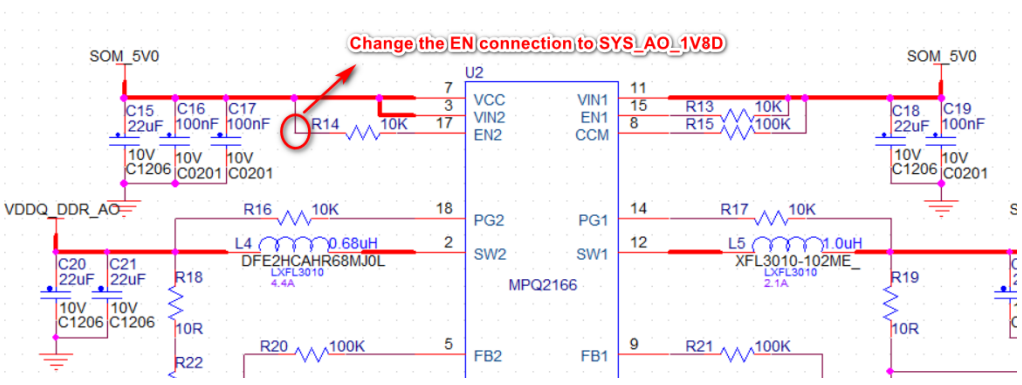

Figure 2-7 VDD1 EN Connection

2. Add extra 47uF capacitor to the output of PF5024 channel 1.

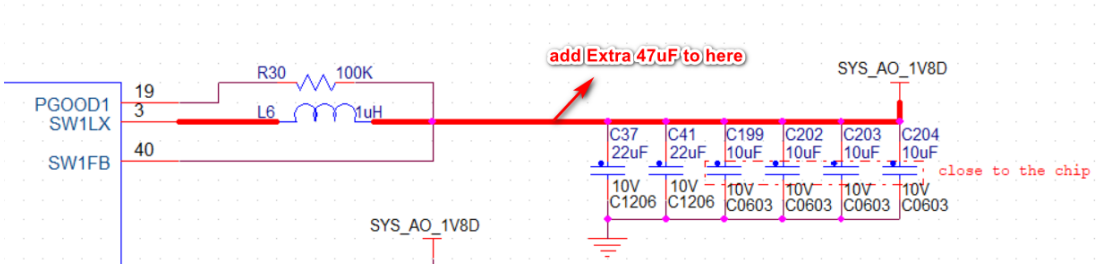

Figure 2-8 Add to VDD1 Extra 47uF Capacitor

After the workaround, the power ramp/off waveform are as the Figure 2-9 and Figure 2-10.

Note: the yellow curve is 1.1V (VDDQ and VDD2), the green curve is 1.8V (VDD1), the red curve is 5V (input to the PMIC).

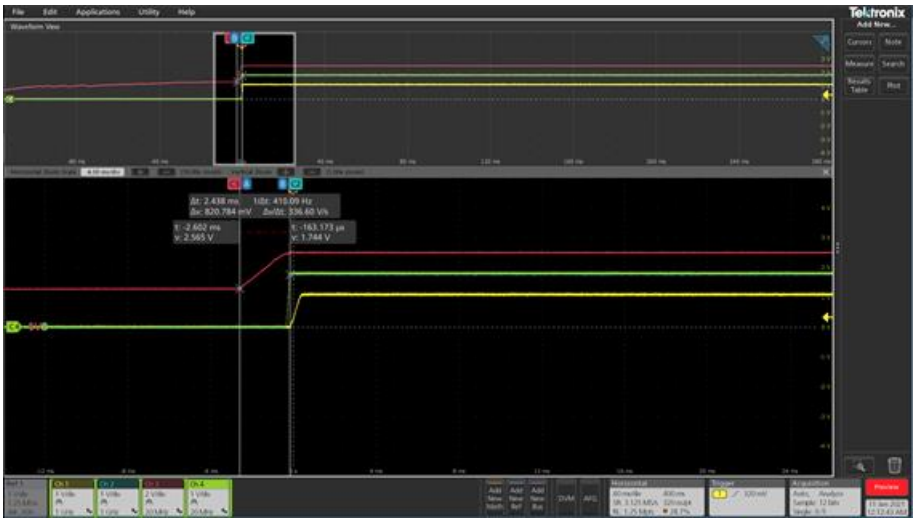

Figure 2-9 Power Ramp after Workaround

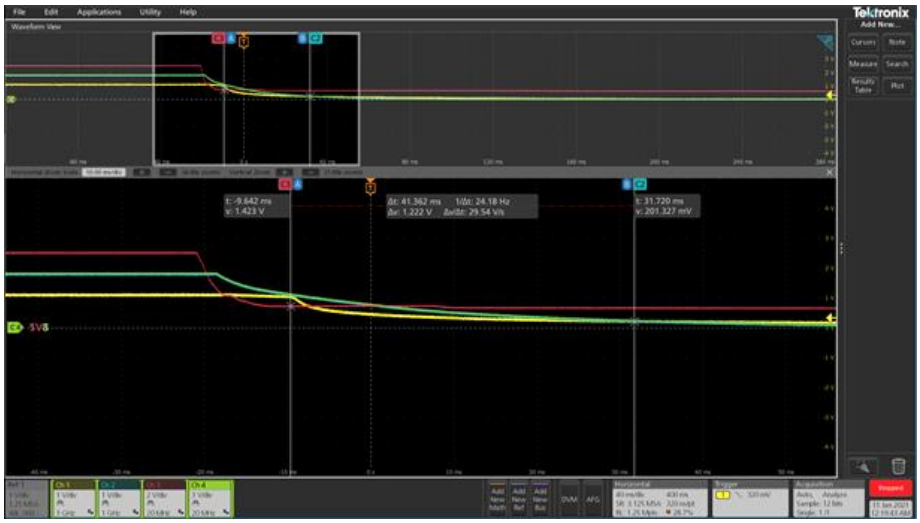

Figure 2-10 Power off after Workaround

2.5 USB Device mode Hot-plug Support

Issue description:

When Journey3 acts as USB device, extra consideration should be taken to support the Hot-plug feature.

USB_VBUS pin is not functional available at the package ball. The 30KΩ pull up resistor is no longer needed, and the VBUS detection is also not available through USB_VBUS pin.

Workaround:

Solution A: use a separate GPIO to detect the VBUS insertion. Please refer to the Figure 2-11 for the detail connection. Dedicated software thread is needed for GPIO status polling.

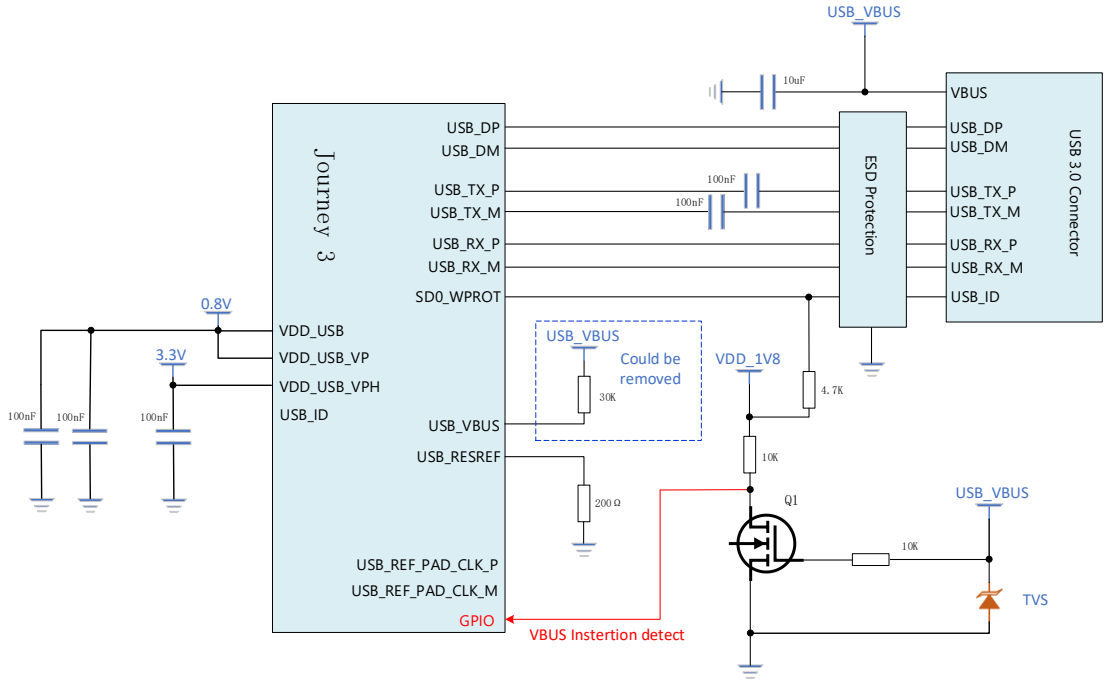

Figure 2-11 VBUS Insertion Detection Solution

Solution B: Use USB_VBUS as enable signal to the Journey3's PMIC output. J3 will not power up without USB_VBUS inserted. This is common in Smart USB Camera scenario. Please refer to the Figure 2-12 for this solution.

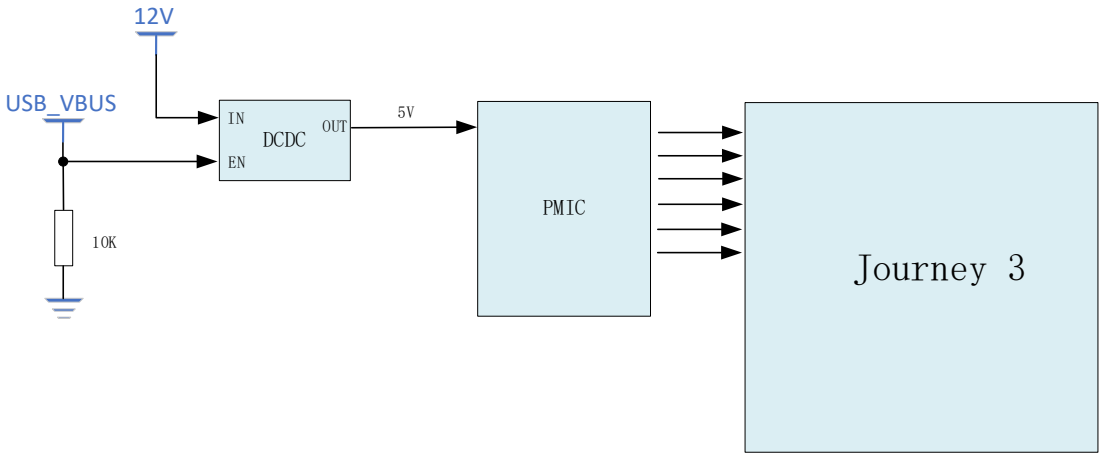

Figure 2-12 USB VBUS Controlled Power up for J3